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Fractal Structures for Low-Resistance Large Area AlGaN/GaN Power Transistors

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***Abstract*—This work introduces a new design approach for the use of fractal structures for low-resistance large area transistors structures. Aspects of layout with adapted current density and high-area utilization are considered. Furthermore the work presents a realization of fractal structures in AlGaN/GaN technology. Both static and dynamic behaviors are characterized. The fabricated devices achieve a breakdown voltage of V_{BR} > 700V and on-state currents of I_D = 40A at V_{GS} = 1V.**

Keywords-fractal design; natural flow system; self similarity; lateral flow structure; gallium nitride

I. INTRODUCTION

GaN-based heterojunction field-effect transistors (HFET) provide outstanding properties for highly-efficient switching converters for photovoltaic and automotive applications. High breakdown voltages can be achieved in the off-state. On the other hand low on-state resistances and high on-state currents for large area transistor structures are possible, because the heterojunction structure induces high electron density and high carrier mobility in the transistor channels. An overview of the topic and the high potential of such GaN devices is published, e.g., in [1]. AlGaN/GaN HFETs are lateral devices. HFETs with low on-state-resistance and large area are usually designed as comb structures with a high number of transistor fingers which are connected in parallel. For large area structures a chip designer should take into account the influence of resistive metallization. Inappropriately designed metallization structures result in inefficient area utilization. Furthermore, the current density appears inhomogeneously on the fingers on unadapted metallization structures. This current crowding effect can affect the performance [2]. The new approach in this work is to use fractal structures for lateral-large area transistors. Fractal branch structures can be found in many examples in nature flow systems, e.g., blood circuits, roots, trees, and watershed [3]. In this approach the resistance of each branch is adapted to the current flow to reach a nearly homogenous flow in metallization and active area.

II. DESIGN OF FRACTAL FLOW STUCTURES

A. Limits of Transistor Finger Structures and Design of Area-Efficent Fractal Metallization Structures

The cross-section structure of a transistor finger determines the behavior in the off-state. Especially GaN-buffer thickness, shape of field plates, and the gate drain distance l_{DS} are the most important design parameters to achieve a certain breakdown voltage. For high breakdown voltages the drain gate distance l_{GD} dominates the overall transistor channel length l_{DS}. In the on-state the channel length l_{DS} and the sheet resistance of the active area $R_{SH\,A}$ determine the lowest possible area-specific resistance $R_{on}A_{\,min} = R_{SH\,A}\,l_{DS}^2$. A challenge in design of large-area lateral transistors is to find an area-efficient metallization structure that approaches this minimum value of $R_{on}A_{\,min}$. In order to get an area-efficient finger design, there are two important design limits which should not be exceeded. The first limit is found in publication [2] to read:

$$W_{crit} = Log_e(3+2\sqrt{2})\sqrt{\frac{l_{MET}\,l_{DS}\,R_{SH\,A}}{2R_{SH\,MET}}}\,. \qquad (1)$$

By exceeding this gate width the resistance of metallization becomes dominant and the value of $R_{on}A$ rises up immediately. The length of the metallization on the drain and source side is denoted with l_{MET}, where $R_{SH\,MET}$ is the sheet resistance of metallization. The second limit is related to the metallization area. The specific resistance of the drain and source metallization is given by: $R'_{MET}=R_{SH\,MET}/l_{MET}$. If $l_{MET} > l_{DS}/2$, the area of metallization becomes larger than the active area. A further reduction of R'_{MET} requires an area-consuming metallization and $R_{on}A$ rise up as well. Therefore the

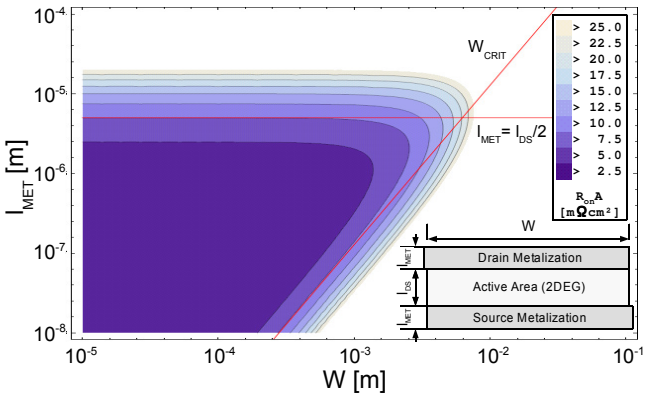

Figure 1. The $R_{on}A$ is plotted versus the gate width W and the length of the metallization l_{MET}. The vaule of $R_{on}A$ can be seen as a figure-of-merit for the area efficency. In the example a drain-source distance of l_{DS}=*10 µm* is given. The sheet resistance of the metalization is $R_{SH\,MET}$ = *0.001 Ω/□* and the sheet resitance of the active area is $R_{SH\,A}$ = *500 Ω/□*. The equations used to calculate $R_{on}A$ can be found in publication [2].

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metallization area should not be larger than the active area.

In Figure 1 the area specific on-state resistance $R_{on}A$ is plotted versus the gate width W and the length of the metallization l_{MET}. The dark blue area shows the range where the specific on-state resistance $R_{on}A$ reaches nearly the lowest possible value $R_{on}A_{min}$. The design parameters in this region lead to an area-efficient design, whereas the red lines mark the two limits were $R_{on}A$ rises up immediately. Thus the dimensions of an area-efficient finger structure are limited by the resistance of metallization. To come to a lower total on-state resistance designers connect fingers in parallel. This leads to the conventional comb structure. With a drain and a source bus metallization a comb structure can be viewed as a next higher order finger structure, as shown in Figure 2. With newly defined finger parameters the two limits are valid again to make an area-efficient design of this higher order finger. Repeating the connection in parallel of higher order fingers leads to a fractal design. But in terms of area efficiency this action results in no benefit, if the sheet resistance of metallization is the same for all higher order. Therefore the sheet resistance should be reduced on each higher order of branch metallization to keep the area efficiency on fractal metallization structures. The reduction of metallization sheet resistance can be realized by increased metallization thickness.

B. Flow Adapted Branching in Fractal Structures

Finger structures with rectangular shaped metallization have inhomogeneous current flow along the metallization and active area. An inhomogeneous current density causes an inhomogeneous power density on the chip, because $P = R \cdot I^2$, and therewith an inhomogeneous thermal heating on the chip. An example of the inhomogeneous flow in a 2nd order finger structure (comb structure) with opposed bond wire interfaces is visualized in Figure 3.b. The current density accumulates on the bond interfaces. Whereas, on the opposite sides on drain and source bus the current density is decreased to nearly zero. The same behavior can be observed on the 1st order transistor fingers as well. A solution to reach a homogeneous flow is to adapt the metallization on each branch interface to its current density. This lead to tapered shaped metallization on finger structures as shown in Figure 3.a.

C. Fractal Approach for Impedance Matching

The design aspects for fractal structures shown above are focused to improve the static on-state of the transistor. However, fractal branching is also a promising approach to improve the switching behavior. Branching can be used for matching impedances between load and active-area of 1st order fingers. Impedance splitting on a branch interface has the relation $Z_{L0}' = Z_{L1}'' \cdot Z_{L2}'' / (Z_{L1}'' + Z_{L2}'')$. The low impedance of the higher order branch is denoted with Z_{L0}', whereas Z_{L1}'' and Z_{L2}'' are the two lower order branches with higher impedances. This is not only advantageous to improve switching behavior at the drain and source; it can also be used to match the low impedance of the gate driver output to the high-impedance of each gate finger. Reflections can be reduced and the switch behavior can be enhanced. However, in switching applications complete matching is not possible, since impedances change together with operation points, but nevertheless a tradeoff can

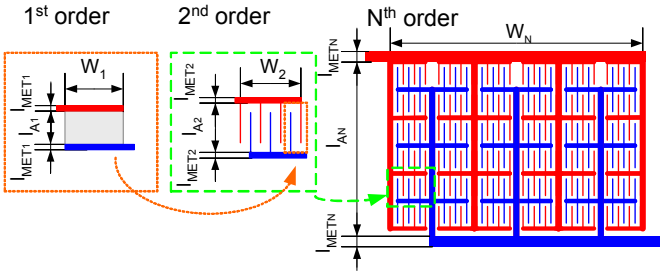

Figure 2. Example of a fractal finger structure for lateral transistor structures. A confentional finger structure serves as a base structure. A parallel connection of a number of fingers results in a comb struture, which can be seen as a 2nd order-finger structure. The parallel connection of the comb struture results in a next higher order-finger structure. Higher order finger structures lead to self-similar structure and these are called fractal.

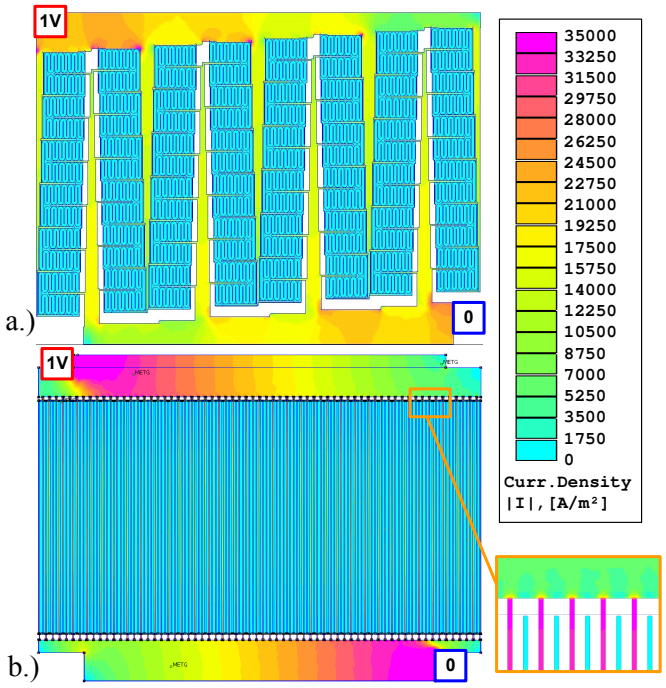

Figure 3. FEM-Simulation for a comparison of the current densities on the chip metallization of two layouts ($A = 4x3\ mm^2$, $l_{GD} = 20\ \mu m$). a.) fractal structure has nearly homogenious current density; b.) conventional comb structure has locally high current densities.

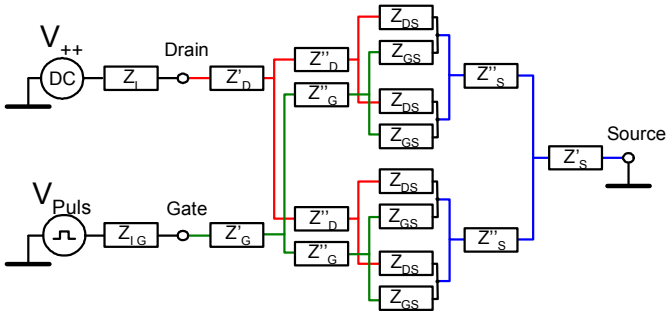

Figure 4. Concept of impedance matching by fractal branch structures.

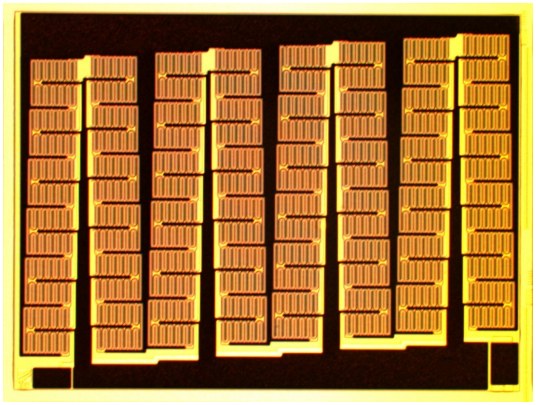

Figure 5. Fractal large-area AlGaN/GaN HFET with total gate width W = 194 mm and chip area 4x3 mm².

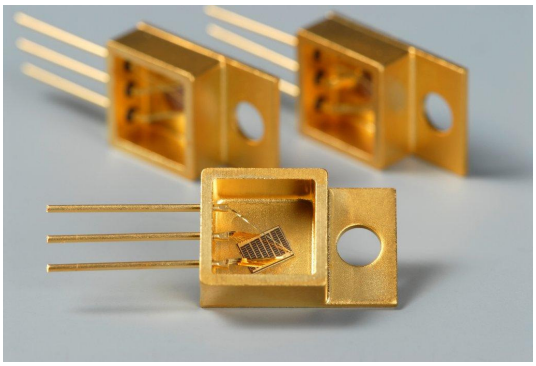

Figure 6. Fractal AlGaN/GaN HFET packaged in a TO220 engineering package.

be found and matching for a critical operation point can be made.

III. Realization of a Low-Resitance Large Area AlGaN/GaN Power Transistor

Within this work a fractal transistor was realized in an AlGaN/GaN technology on 3" SiC substrates [4]. Chip dimensions are $A_{total} = 4x3\ mm^2$. The transistor has a total gate width $W = 194\ mm$, the drain to gate distance is $L_{GD} = 20\ \mu m$, gate length is $L_G = 2\ \mu m$, and gate to source distance amounts to $L_{GS} = 2\ \mu m$. The mask layout is developed by parameterized cells using the scripting programming language SKILL as part of the electronic design software Cadence [5]. In order to save chip area the 2nd order finger structures is realized by meander gates. To get a homogenous current flow and to get a uniform power density on the chip area the 3th and 4th order drain and source metallization are tapered shaped. The chip is soldered and packaged into a TO220 engineering package and pads are connected via multiwire gold bonding.

IV. Measurement Results

A. Characterization of the Static Behavior

The static behavior of the fabricated fractal transistor was characterized by on-wafer measurements. In the off-state

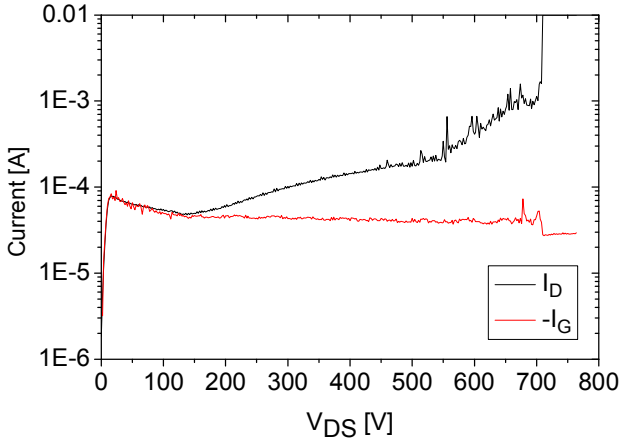

Figure 7. Off-state breakdown measurement on a fractal large-area AlGaN/GaN HFET. The device was measured on-wafer using Fluorinert™ to prevent breakdown through atmosphere.

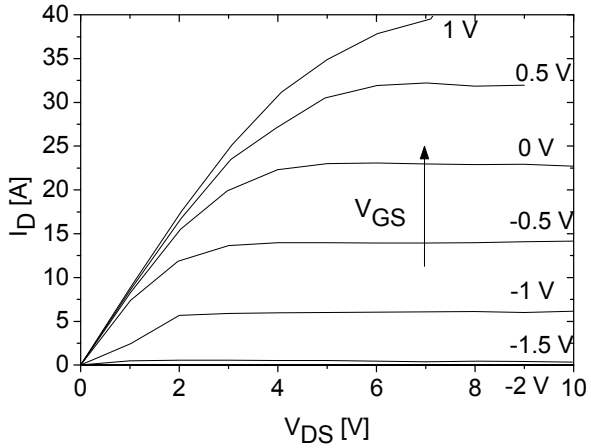

Figure 8. On-state current and resistance measurement on a fractal large-area AlGaN/GaN HFET. A 4 - point measurement methode was used to remove influence of parasitic resistances of the setup.

breakdown voltages with values higher than $V_{BR} = 700\ V$ are measured with drain leakage currents below $I_{D\_leak} \leq 5\ \mu A/mm$ and gate leakage currents below $I_{G\_leak} < 0.5\ \mu A/mm$. In the on-state currents up to $I_{D\,Max} = 40\ A$ are measured at a corresponding gate voltage of $V_{GS} = 1\ V$. In 4 - point measurements the devices achieved on-state resistance of $R_{on} = 110\ m\Omega$ at a corresponding drain current of $I_D = 10\ A$. The measurements in this work were made at room temperature. The threshold voltage of the devices is $V_{TH} = -1.6\ V$. The sheet resistance of the active region was measured on a TLM (Transfer Length Method) structures with a value of about $R_{SH\,A} = 650\ \Omega/\square$.

B. Characterization of the Dynamic Behavior

A test circuit was built to characterize gate charge and the switching behavior of the devices. The circuit is shown in Figure 9. The gate is driven by a pulse generator, a power MOSFET driver *IXYS DEIC420* and a gate resistor R_G between driver output and gate. A value of $R_G = 51\ \Omega$ is chosen to characterize the gate charge behavior to monitor charging slope and to detect a stable gate current. The driver is biased with a

differential voltage supply $V_{DRV+} = 1\ V$ and $V_{DRV-} = -3\ V$. At the drain there is a real load resistor with a value of $R_L = 56\ \Omega$. Dimensions between high voltage supply pad at the load resistor and GaN transistor source contact are chosen to be small to prevent induction peaks by parasitic inductances. Additional freewheeling diodes are in use.

The switching behavior of the falling and the rising edge are shown in Figure 10. The current is determined by using differential voltage over the resistors, thus $I_G = (V_{pls}-V_{GS})/R_G$ and $I_D = (V_{++}-V_{DS})/R_L$. The gate charge can be calculated by calculating the integral $Q_G = \int I_G(t)\,dt$, and visualized as typical gate charge curve with gate voltage versus gate charge, shown in Figure 11. Compared to Si-devices, wide bandgap devices achieve a lower product of on-state resistance and gate charge,

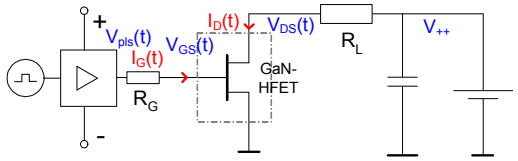

Figure 9. Test circuit to charaterize the switching behavior and to monitor gate charge behaivor.

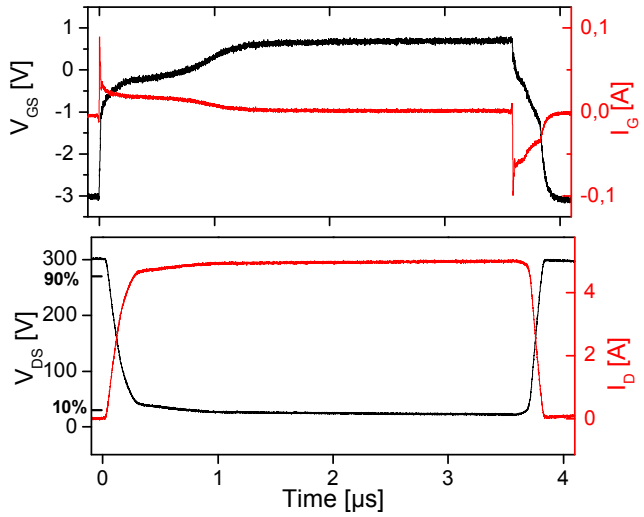

Figure 10. Pulse shape at gate and drain of the fractal AlGaN/GaN HFETs descriped in this work. A gate resistor of $R_G = 51\ \Omega$ between driver and gate is chosen. On the drain a real load of $R_G = 56\ \Omega$ is connected.

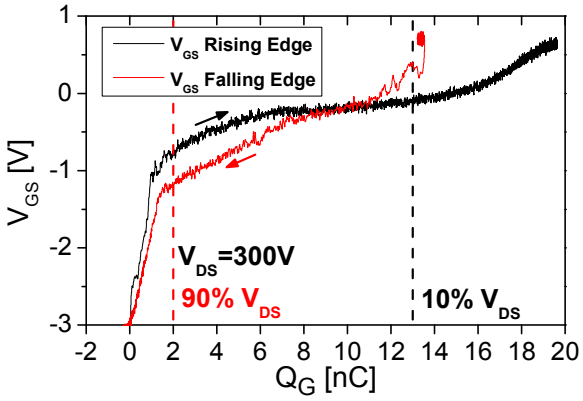

Figure 11. Gate charge curve showing gate voltage V_{GS} vs. gate charge I_G. The gate charge is shown for the rising and the falling edge.

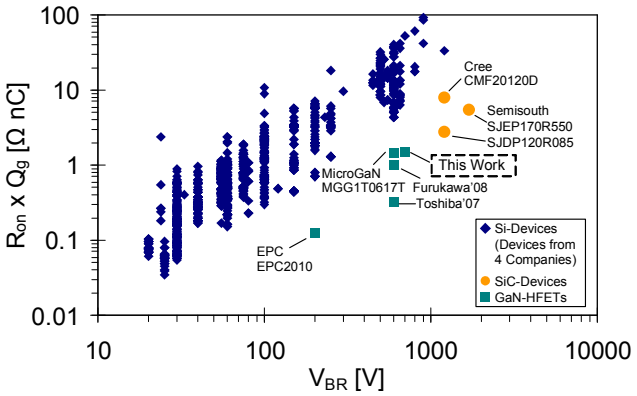

Figure 12. The product of the on-state resistance and the gate charge of transistors are compared for different technologie and ploted vs. breakdown voltage.

shown in Figure 12. This product $R_{on}Q_G$ is deemed to be a figure of merit for power transistors for efficient and compact voltage converter [6].

Conclusion

This work introduces a new approach to use fractal designs for large area, lateral transistors structures. The efficiency limits of finger structures are presented, and a design method for area-efficient fractal structures derived. Aspects for layouts with adapted current density and the use of fractal structures for impedance matching is considered. Furthermore the work shows the realization of the fractal design. The structure is fabricated using an AlGaN/GaN technology and packaged in a TO220 package. The characterization of the static and dynamic behavior is presented. We achieve high breakdown voltages higher than $V_{BR}>700V$, high on-currents $I_D=40A$, and a $R_{on}Q_G$ value which is more than factor of three smaller than comparable, commercial Si-devices.

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